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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,701	06/24/2003	Ching-Fa Yeh	BHT-3230-56	7550

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TROXELL LAW OFFICE PLLC
SUITE 1404
5205 LEESBURG PIKE
FALLS CHURCH, VA 22041

EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,701	YEH ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 6/24/03. Currently, claims 1-7 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 10/20/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

1. The drawings are objected to under 37 CFR 1.83(b) because they are incomplete. 37 CFR 1.83(b) reads as follows:

> When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

For example, in figure 2, "?" and "??" are shown in the drawings, not the references numbers described in the specification with regards to this particular figure.

2. Figure 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted

by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification

are: on page 6, lines 4-7, the statement "to form a stop layer of silicon film dry etching after step d) process, a thermal insulating layer of laser annealing or a hard mask of the removal of polysilicon spacer after recrystallization;" is unclear in its meaning. In addition, on lines 8-13, the statement "forming amorphous silicon film 3 by photoresist of hardmask on the low temperature polycrystalline silicon thin film transistor (LTPS-TFT) as a active layer and then using a solution of silicon dioxide 6 of wet isotropic etching to slightly go toward to slightly go toward inner etching of the buffer oxide 2 before or after removal of the hard mask." is unclear in its meaning. In general, there are numerous errors with regards to grammar and spelling. The specification appears to be the result of a direct translation. Correction is required.

4. A substitute specification including the claims is required pursuant to 37 CFR 1.125(a) because there are numerous errors with regards to clarity, grammar, and spelling.

A substitute specification must not contain new matter. The substitute specification must be submitted with markings showing all the changes relative to the immediate prior version of the specification of record. The text of any added subject matter must be shown by underlining the added text. The text of any deleted matter must be shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The text of any deleted subject matter must be shown by being placed within double brackets if strike-through cannot be easily perceived. An accompanying clean version (without markings) and a statement that the substitute specification contains no new matter must also be supplied. Numbering the paragraphs of the specification of record is not considered a change that must be shown.

Claim Objections

Claims 1 and 7 are objected to because of the following informalities: on line 6, of claim 1 "d)depositing" should be "d) depositing". On line 22, claim 1, "shap" should be "shape". On line 3, claim 7, "sel cting" should be "selecting". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In lines 7-10, of claim 1, it is indefinite as to what is meant by the limitation, "...dry etching after step d) process, a thermal insulating layer of laser annealing or a hard mask of the removal of polysilicon spacer after recrystallization;" specifically, what is meant by "a thermal insulating layer or a hard mask of the removal of polysilicon spacer after recrystallization;" For examination purposes of the merits, the examiner will assume that the "low-temperature oxide" is being dry etched. Correction and clarification are required.

In lines 11-15, of claim 1, it is indefinite as to what is meant by the limitation, "e) forming amorphous silicon film by photoresist of hard mask on the low temperature polycrystalline thin film transistor (LTPS-TFT) as a active layer, and then using a solution of silicon dioxide of wet isotropic etching to slightly go toward in etching of said buffer oxide

before or after the removal of said hard mask;" Specifically, what is meant by "forming amorphous silicon film by photoresist of hard mask". As stated in the claim and the specification, the amorphous film is deposited on the buffer oxide. How is the amorphous silicon film formed by the photoresist? In addition, does the solution for wet isotropic etching include silicon dioxide? How is that possible? Especially since conventionally wet etching techniques may be used to etch silicon dioxide. Furthermore, is the silicon dioxide an additional layer insulating layer or does this represent the buffer oxide? For examination purposes on the merits, the Examiner will assume that the silicon dioxide is the buffer layer, and that the photoresist is used as a hard mask. Correction and clarification are required.

Thorough revision of the claims is required as they appear to result form direct translation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. US Patent 5,589,406 in view of Hasegawa Patent Application Publication US 2004/0026738, in so far as the Examiner can interpret the disclosure and claimed invention.

Kato discloses the semiconductor method substantially as claimed. See figures 1-7 especially, Table 1, and corresponding text, where Kato teaches a method for fabrication of

polycrystalline silicon thin film transistors, pertaining to claim 1, comprising the steps of: a) substrate **100** b) a buffer oxide (Table 1; col. 11, lines 1-8, insulating substrate) formed on said substrate; c) depositing a amorphous silicon film (1 in Table 1) on said buffer oxide (col. 7, lines 55-67; col. 10, lines 56-67; col. 11, lines 1-31); d) depositing a low-temperature oxide (4 in Table 1) on said amorphous silicon film, wherein said low temperature oxide is employed to form a stop layer (col. 10, lines 56-67; col. 11, lines 1-31), and after step d) performing a dry etching process that includes using the photoresist as a hard mask to form an active layer for a temperature polycrystalline silicon thin film transistor (LTPS-TFT) (col. 10, lines 56-67; col. 11, lines 1-31); e) then using a solution to etch the buffer oxide by wet isotropic etching to slightly go toward inner etching of said buffer oxide before or after the removal of said hard mask (col. 10, lines 56-67; col. 11, lines 1-31); f) and then forming large silicon grain structures of said active layer by recrystallization of high-energy continuous wavelength laser or recrystallization of excimer laser annealing on dog-bone shape active layer (figure 5; col. 10, lines 1-33). In addition, Kato teaches, pertaining to claim 7, wherein said the step f) forming recrystallization active layer by selecting form the group consisting of excimer laser annealing (ELA), solid phase crystallization (SPC) or metal-induced lateral crystallization (MILC), and then forming said polysilicon spacer on either side of said active layer on the thin film transistor (TFT) or silicon-on-insulator metal oxide semiconductor field effect transistor (SOI-MOSFET) (col. 1, lines 65-67; and col. 2, lines 1-48; col. 9, lines 49-67).

However, Kato fails to show, pertaining to claim 1, f) depositing another amorphous silicon film by connecting said active layer, and then forming said polysilicon spacer by dry etching behind either side of said active layer of the low temperature polycrystalline silicon thin

film transistor (LTPS-TFT), and then forming large silicon grain structures of said active layer by recrystallization of high-energy continuous wavelength laser or recrystallization of excimer laser annealing on dog-bone shape active layer. In addition, Kato fails to show, pertaining to claim 2, wherein said polysilicon spacer is selected from the group consisting of polycrystalline silicon film and amorphous silicon film. Also, Kato fails to show, pertaining to claim 3, wherein said polysilicon spacer of step f) form in either side of said active layer of selecting from the group consisting of thin film transistor (TFT) and silicon-on-insulator metal oxide semiconductor field effect transistor (SOI-MOSFET) in the low temperature or high temperature process. Kato fails to show, pertaining to claim 4, further comprising under either side of said active layer. In addition, Kato fails to show, pertaining to claim 5, wherein said polysilicon spacer step f) by recrystallization of high-energy continuous wavelength laser or recrystallization of excimer laser annealing on dog-bone shape active layer is to generate temperature gradient. Finally, Kato fails to show, pertaining to claim 6, where said polysilicon spacer replace dielectric material with oxide, nitride, and metal oxide, etc. and metal material with aluminum (al), wolfram (W), molybdenum (Mo) and chromium (Cr), etc.

Hasegawa teaches, in figures 1-7, and corresponding text, a polycrystalline CMOS device, that includes the use of a second polycrystalline silicon formed on a silicon active layer to create side spacers for the active layer (figures 5A-5E; paragraphs [0040-0041]).

It would have been obvious to one of ordinary skill in the art to substitute, pertaining to claim 1, f) depositing another amorphous silicon film by connecting said active layer, and then forming said polysilicon spacer by dry etching behind either side of said active layer of the low temperature polycrystalline silicon thin film transistor (LTPS-TFT), and then forming large

silicon grain structures of said active layer by recrystallization of high-energy continuous wavelength laser or recrystallization of excimer laser annealing on dog-bone shape active layer. In addition, it would have been obvious to one or ordinary skill in the art to substitute, pertaining to claim 2, wherein said polysilicon spacer is selected from the group consisting of polycrystalline silicon film and amorphous silicon film; also, it would have been obvious to one of ordinary skill in the art to substitute, pertaining to claim 3, wherein said polysilicon spacer of step f) form in either side of said active layer of selecting from the group consisting of thin film transistor (TFT) and silicon-on-insulator metal oxide semiconductor field effect transistor (SOI-MOSFET) in the low temperature or high temperature process; it would have been obvious to one of ordinary skill in the art to substitute, pertaining to claim 4, further comprising under either side of said active layer; in addition, It would have been obvious to one of ordinary skill in the art to substitute, pertaining to claim 5, wherein said polysilicon spacer step f) by recrystallization of high-energy continuous wavelength laser or recrystallization of excimer laser annealing on dog-bone shape active layer is to generate temperature gradient; finally, it would have been obvious to one of ordinary skill in the art to substitute, pertaining to claim 6, where said polysilicon spacer replaces dielectric material with oxide, nitride, and metal oxide, etc. and metal material with aluminum (al), wolfram (W), molybdenum (Mo) and chromium (Cr), etc, in the method of Kato, according to the teachings of Hasegawa, with the motivation, that, the resistance depends on the crystal grain diameter, grain boundaries and on film thickness, of the polycrystalline silicon. Therefore, it would be obvious to one of ordinary skill in the art use a polysilicon spacer formed on the on the active layer, for the purpose of adjusting the crystal grain diameter and grain boundaries of the active layer of a low temperature polycrystalline silicon

thin film transistor (LTPS-TFT). In addition, it would be obvious to form large silicon grain structures of the active layer by recrystallizing with a high-energy continuous wavelength laser or with an excimer laser annealing on a dog-bone shape active layer, resulting in a uniform crystal grain diameter and grain boundaries on the active layers, for the purpose of eliminating current leakage, resulting in a more efficient semiconductor device. Also, it would have been obvious to substitute the polysilicon spacer with for example, a dielectric material containing an oxide, to possibly reduce the active layer region thus creating an additional isolation between of active layers of additional semiconductor devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
December 8, 2004

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812